What is claimed is:

1. A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions where are respectively contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively contact with the pair of impurity layers, wherein bottom surfaces of the pair of metallic silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among

stoichiometaric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequity:

$$(X / Y) > (X0 / Y0).$$

2. The field effect transistor according to claim 1, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

3. A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on an insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions where are respectively contact with the channel region in the source region and the drain region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively contact with the pair of impurity layers, wherein bottom surfaces of the pair of cobalt silicide layers extend to bottom surfaces of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

4. The field effect transistor according to claim 3, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

5. A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on the insulating layer, wherein the semiconductor layer includes the channel region defined by the source region and the drain region;

a pair of impurity layers formed into regions where are respectively contact with the channel region in the source region and the drain region; and

a pair of metallic silicide layers respectively formed in the source region and the drain region, wherein the pair of metallic silicide layers are respectively contact with the pair of impurity layers, wherein the pair of metallic silicide layers have a thickness which is equal to or more than 80% thickness of from the upper surface of the metallic silicide layers to the bottom surface of the semiconductor layer;

wherein the metallic silicide layers are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometaric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequity:

$$(X / Y) > (X0 / Y0).$$

6. The field effect transistor according to claim 5, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

7. A field effect transistor including a gate electrode and a channel region defined by a source region and a drain region, comprising:

an insulating layer;

a semiconductor layer formed on an insulating layer, wherein the semiconductor layer includes the channel region therein;

a pair of impurity layers formed in regions where are respectively contact with the channel region in the source region and the drain region; and

a pair of cobalt silicide layers respectively formed in the source region and the drain region, wherein the pair of cobalt silicide layers are respectively contact with the pair of impurity layers, wherein the pair of cobalt silicide layers has a thickness which is equal to or more than 80% thickness of from the upper surface of the cobalt silicide layers to the bottom surface of the semiconductor layer;

wherein the cobalt silicide layers are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α $(1<\alpha<2)$.

8. The field effect transistor according to claim 7, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

9. A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first impurity layer and the first metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide

layer, wherein the second impurity layer and the second metallic silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity region and the second impurity,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometaric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequity:

$$(X / Y) > (X0 / Y0).$$

10. The field effect transistor according to claim 9, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

11. A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed

in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first impurity layer and the first cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second impurity layer and the second cobalt silicide layer are formed so as to reach the insulating layer through the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity region and the second impurity, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α $(1<\alpha<2)$.

12. The field effect transistor according to claim 11, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

13. A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed

in the semiconductor layer, comprising:

the source region including a first impurity layer and a first metallic silicide layer, wherein the first metallic silicide layer have a thickness which is equal to or more than 80% thickness of from the upper surface of the first metallic silicide layer to the bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second metallic silicide layer, wherein the second metallic silicide layer have a thickness which is equal to or more than 80% thickness of from the upper surface of the second metallic silicide layer to the bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity region and the second impurity,

wherein the first metallic silicide layer and the second metallic silicide layer are composed of refractory metal and silicon, and

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometaric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following

inequity:

$$(X / Y) > (X0 / Y0).$$

14. The field effect transistor according to claim 13, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

15. A field effect transistor formed in a semiconductor layer located on an insulating layer, the field effect transistor having a source region and a drain region formed in the semiconductor layer, comprising:

the source region including a first impurity layer and a first cobalt silicide layer, wherein the first cobalt silicide layer have a thickness which is equal to or more than 80% thickness of from the upper surface of the first cobalt silicide layer to the bottom surface of the semiconductor layer; and

the drain region including a second impurity layer and a second cobalt silicide layer, wherein the second cobalt silicide layer have a thickness which is equal to or more than 80% thickness of from the upper surface of the second cobalt silicide layer to the bottom surface of the semiconductor layer;

wherein the first impurity layer is located so as to face to the second impurity layer,

wherein a channel between the source region and the drain region is defined by the first impurity region and the second impurity, and

wherein the first cobalt silicide layer and the second cobalt silicide layer are composed of cobalt and silicon, wherein a ratio of cobalt to silicon is one to α ($1<\alpha<2$).

16. The field effect transistor according to claim 15, wherein said field effect transistor has a depletion layer which expands to the bottom surfaces of the source region and the drain region when a voltage is supplied to the gate electrode thereof.

17. A method for manufacturing a field effect transistor, comprising:

preparing a substrate having a semiconductor layer formed on an insulating layer, wherein the semiconductor layer includes silicon;

forming a gate electrode on a channel region in the semiconductor layer through a gate insulating film;

forming insulating sidewalls on side surfaces of the gate electrode;

forming a pair of impurity layers adjacent to the channel region in the semiconductor layer;

forming a refractory metallic film on the substrate formed the gate electrode on the channel region in the semiconductor layer through the gate insulating film;

exposing the refractory metallic film to a first heat treatment so as to form metallic silicide layers containing refractory metal and silicon; and

exposing the first heat-treated metallic silicide layers to a second heat treatment;

wherein a ratio of the metal to the silicon in the metallic silicide layers is X to Y, a ratio of the metal to the silicon of metallic silicide having the lowest resistance among stoichiometaric metallic silicides is X0 to Y0, and X, Y, X0 and Y0 satisfy the following inequity:

$$(X / Y) > (X0 / Y0).$$

18. The method for the field effect transistor according to claim 17, wherein the bottom surface of the second heat-treated metallic silicide layers reaches the upper surface of the insulating layer.

19. The method for the field effect transistor according to claim 17, wherein the second heat-treated metallic silicide layers have a thickness which is equal to or more 80% thickness of from the upper surface of the second heat-treated metallic silicide layers to the upper surface of the insulating layer.

20. A method for manufacturing a field effect transistor, comprising:

preparing a substrate having a semiconductor layer formed on an insulating layer,

wherein the semiconductor layer includes silicon;

forming a gate electrode on a channel region in the semiconductor layer through a gate insulating film;

forming insulating sidewalls on side surfaces of the gate electrode;

forming a pair of impurity layers adjacent to the channel region in the semiconductor layer;

forming a cobalt film on the substrate formed the gate electrode on the channel region in the semiconductor layer through the gate insulating film;

exposing the cobalt film to a first heat treatment so as to form cobalt silicide layers containing the cobalt and silicon;

exposing the first heat-treated cobalt silicide layers to a second heat treatment, wherein a ratio of cobalt to silicon in the second heat-treated cobalt silicide layers satisfies one to α $(1<\alpha<2)$.

21. The method for the field effect transistor according to claim 20, wherein the bottom surface of the second heat-treated metallic silicide layers reaches the upper surface of the insulating layer.

22. The method for the field effect transistor according to claim 20, wherein the

second heat-treated cobalt silicide layers have a thickness which is equal to or more 80% thickness of from the upper surface of the second heat-treated cobalt silicide layers to the upper surface of the insulating layer.